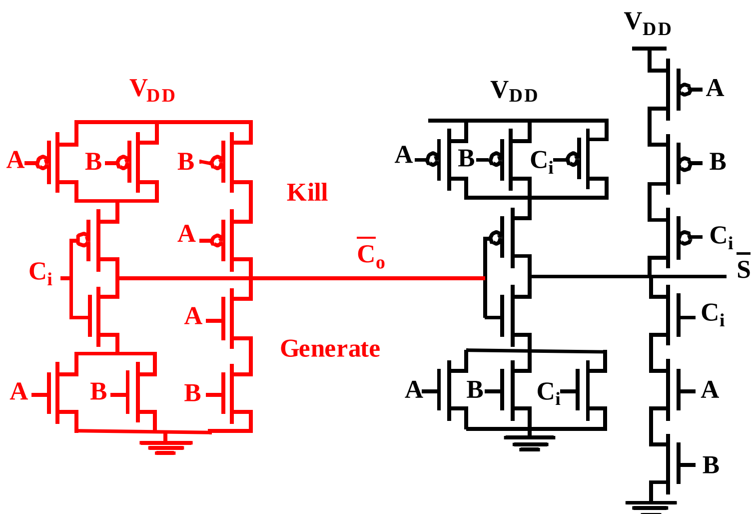
ENGR 848 Course Project
Designing a 4-bit Ripple carry adder in 90nm CMOS

1. Design a full-adder in ComosSE tool and size transistors to **minimize** the critical delay (Ci to /Co). To measure proper delay, you need to connect /Co to Ci of the following same full adder as the load. For non-critical transistors use minimum size to **minimize** power. Measure carry propagation delay (Ci to /Co) and power dissipation of the circuit for a continuous switching of Ci when the full adder is in the carry propagation mode (A=1, B=0, and Ci switching at 1 Ghz).



2. After optimizing the design of a single full adder, cascade 4 of these full adders to implement a 4-bti ripple carry adder (using the idea of mirror ripple carry adder). Use inverters where necessary to generate the right polarity of input and output signals. Use hierarchical schematic design approach to organize your schematic. Measure the critical delay of the ripple carry adder and the power of the ripple carry adder for the input carry switching constantly and the adder being in the carry propagation state (A_i=1, B_i=0, and C_{i0} switching at 1 Ghz).

3. Implement the layout of a single full adder and pass DRC and LVS on it. Try to minimize your layout area. How much is the area?

4. Implement the layout of the 4-bit ripple carry adder by cascading the layouts of the individual full-adders and inserting required inverters. Pass DRC and LVS on it. How much is the total area?

5. Extract the netlist of your ripple carry adder layout with parasitics and rum simulation on it to measure the critical delay and power dissipation for the same input pattern as in 2. Compare you post layout results with your pre-layout results.

6. Quantify the quality of your design as the product of total Area (in um^2), power (in uW), and delay (in pS). The samller this quantity, the better.